# **DELTA MODULATION**

PREPARATION	122
principle of operation	122
block diagram	122
step size calculation	124
slope overload and granularity	124
slope overload	124
granular noise	125
noise and distortion minimization	126
EXPERIMENT	126
setting up	126
slope overload	129
the ADAPTIVE CONTROL signal	129
the output	130
complex message	131
TUTORIAL QUESTIONS	132
APPENDIX	133
a 'complex' message	133

Delta modulation Vol D1, ch 13, rev 1.0 - 121

#### **DELTA MODULATION**

**ACHIEVEMENTS:** an introduction to the basic delta modulator; to observe effects of step size and sampling clock rate change; slope overload and granular noise.

**PREREQUISITES:** some exposure to the principles of delta modulation in course work

ADVANCED MODULES: DELTA MODULATION UTILITIES, WIDEBAND TRUE RMS METER

### **PREPARATION**

# principle of operation

Delta modulation was introduced in the 1940s as a simplified form of pulse code modulation (PCM), which required a difficult-to-implement analog-to-digital (A/D) converter.

The output of a delta modulator is a bit stream of samples, at a relatively high rate (eg, 100 kbit/s or more for a speech bandwidth of 4 kHz) the value of each bit being determined according as to whether the input message sample amplitude has increased or decreased relative to the previous sample. It is an example of differential pulse code modulation (DPCM).

### block diagram

The operation of a delta modulator is to periodically sample the input message, to make a comparison of the current sample with that preceding it, and to output a single bit which indicates the sign of the difference between the two samples. This in principle would require a sample-and-hold type circuit.

De Jager (1952) hit on an idea for dispensing with the need for a sample and hold circuit. He reasoned that if the system *was* producing the desired output then this output could be sent back to the input and the two analog signals compared in a comparator. The output is a delayed version of the input, and so the comparison is in effect that of the current bit with the previous bit, as required by the delta modulation principle.

Figure 1 illustrates the basic system in block diagram form, and this will be the modulator you will be modelling.

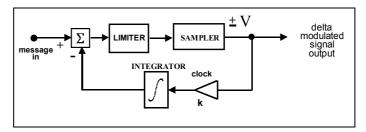


Figure 1: basic delta modulator

The system is in the form of a feedback loop. This means that its operation is not necessarily obvious, and its analysis non-trivial. But you can build it, and confirm that it does behave in the manner a delta modulator should.

The system is a continuous time to discrete time converter. In fact, it is a form of analog to digital converter, and is the starting point from which more sophisticated delta modulators can be developed.

The sampler block is clocked. The output from the sampler is a bipolar signal, in the block diagram being either  $\pm V$  volts. This is the delta modulated signal, the waveform of which is shown in Figure 2. It is fed back, in a feedback loop, via an integrator, to a summer.

The integrator output is a sawtooth-like waveform, also illustrated in Figure 2. It is shown overlaid upon the message, of which it is an approximation.

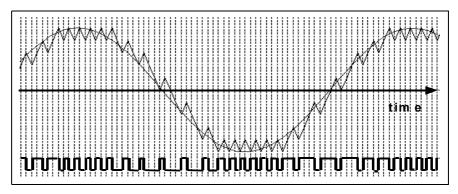


Figure 2: integrator output superimposed on the message with the delta modulated signal below

The sawtooth waveform is subtracted from the message, also connected to the summer, and the difference - an error signal - is the signal appearing at the summer output.

An amplifier is shown in the feedback loop. This controls the loop gain. In practice it may be a separate amplifier, part of the integrator, or within the summer. It is used to control the size of the 'teeth' of the sawtooth waveform, in conjunction with the integrator time constant.

When analysing the block diagram of Figure 1 it is convenient to think of the summer having unity gain between both inputs and the output. The message comes in at a fixed amplitude. The signal from the integrator, which is a sawtooth approximation to the message, is adjusted with the amplifier to match it as closely

as possible. You will be able to see this when you make a model of the system of Figure 1.

#### step size calculation

In the delta modulator of Figure 1 the output of the integrator is a sawtooth-like approximation to the input message. The teeth of the saw must be able to rise (or fall) fast enough to follow the message. Thus the integrator time constant is an important parameter.

For a given sampling (clock) rate the step *slope* (volt/s) determines the *size* (volts) of the step within the sampling interval.

Suppose the amplitude of the rectangular wave from the sampler is  $\pm V$  volt. For a change of input sample to the integrator from (say) negative to positive, the change of integrator output will be, after a clock period T:

$$output = \frac{2kVT}{RC} \ volt \qquad ...... 1$$

where k is the gain of the amplifier preceding the integrator (as in Figure 1).

Answer Tutorial Questions 1 and 2 before attempting the experiment. You can later check your answer by measurement.

### slope overload and granularity

The binary waveform illustrated in Figure 2 is the signal transmitted. This is the delta modulated signal.

The integral of the binary waveform is the sawtooth approximation to the message.

In the experiment entitled *Delta demodulation* (in this Volume) you will see that this sawtooth wave is the primary output from the demodulator at the receiver.

Lowpass filtering of the sawtooth (from the demodulator) gives a better approximation to the message. But there will be accompanying noise and distortion, products of the approximation process at the modulator.

The unwanted products of the modulation process, observed at the receiver, are of two kinds. These are due to 'slope overload', and 'granularity'.

### slope overload

This occurs when the sawtooth approximation cannot keep up with the rate-ofchange of the input signal in the regions of greatest slope.

The step size is reasonable for those sections of the sampled waveform of small slope, but the approximation is poor elsewhere. This is 'slope overload', due to too small a step.

Slope overload is illustrated in Figure 3.

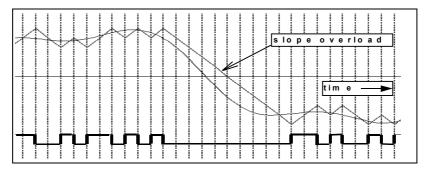


Figure 3: slope overload

To reduce the possibility of slope overload the step size can be increased (for the same sampling rate). This is illustrated in Figure 4. The sawtooth is better able to match the message in the regions of steep slope.

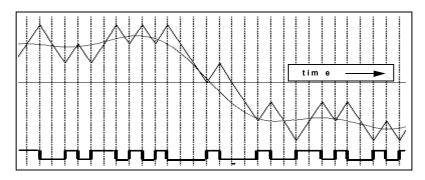


Figure 4: increased step size to reduce slope overload

An alternative method of slope overload reduction is to increase the sampling rate. This is illustrated in Figure 5, where the rate has been increased by a factor of 2.4 times, but the step is the same size as in Figure 3.

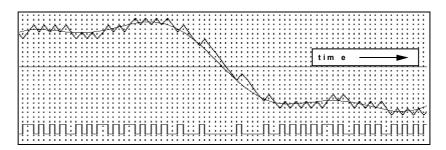


Figure 5: increased sampling rate to reduce slope overload

### granular noise

Refer back to Figure 3. The sawtooth follows the message being sampled quite well in the regions of small slope. To reduce the slope overload the step size is increased, and now (Figure 4) the match over the regions of small slope has been degraded.

The degradation shows up, at the demodulator, as increased quantizing noise, or 'granularity'.

#### noise and distortion minimization

There is a conflict between the requirements for minimization of slope overload and the granular noise. The one requires an increased step size, the other a reduced step size. You should refer to your text book for more discussion of ways and means of reaching a compromise. You will meet an example in the experiment entitled *Adaptive delta modulation* (in this Volume).

An optimum step can be determined by minimizing the quantizing error at the summer output, or the distortion at the demodulator output.

### **EXPERIMENT**

The block diagram of Figure 1 is modelled with a DELTA MODULATION UTILITIES module, an ADDER, and both of the BUFFER AMPLIFIERS.

You should obtain a DELTA MODULATION UTILITIES module, and read about it in the *TIMS Advanced Modules User Manual*. This module contains three of the elements of the block diagram, namely the LIMITER, SAMPLER, and INTEGRATOR.

The SUMMER block is modelled with an ADDER, both gains being set to unity.

The amplifier preceding the INTEGRATOR in the feedback loop is modelled by a *pair* of BUFFER AMPLIFIERS connected in cascade. These amplifiers both invert, so the combination will be non-inverting - as required.

If the ADDER gains are left fixed at unity, and the message and sampling rates fixed, the only variables to be investigated are the INTEGRATOR time constant, and the gain k of the amplifier (the two BUFFERS in cascade) in the feed back loop.

### setting up

T1 obtain and examine a DELTA MODULATOR UTILITIES module. Read about it in the TIMS Advanced Modules User Manual. Before plugging it in set the on-board switches to give an intermediate INTEGRATOR time constant (say SW2A to ON, and SW2B to OFF). Start with no division of the 100 kHz sample clock (front panel toggle switch up to 'CLK').

**T2** plug in the ADDER and DELTA MODULATION UTILITIES module.

T3 use a sinewave to set both of the ADDER gains close to unity. Do not change these for the duration of the experiment.

- T4 use a sinewave to set both of the BUFFER AMPLIFIER gains to about unity (they are connected in series to make a non-inverting amplifier). Either one or both of these will be varied to make adjustments to the step size during the course of the experiment.
- TTL signal from the MASTER SIGNALS module as the clock for the Sampler, and the 2 kHz message for the sinusoidal message to be sampled. The message (2.083 kHz) is a sub-multiple of the 100 kHz sample clock. This helps to obtain text-book like oscilloscope displays.

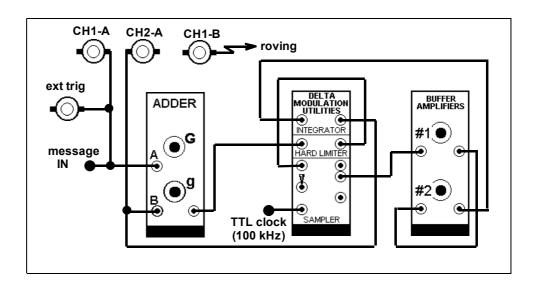


Figure 6: the delta modulator; a model of Figure 1

**T6** use the 2 kHz message as the 'ext. trig' signal to the oscilloscope. The signals of immediate interest are the two inputs to the SUMMER, shown connected to CH1-A and CH2-A. Use CH1-B to explore other signals.

You will now set up the modulator for 'acceptable performance'. This means that the INTEGRATOR output should be a reasonable approximation to the message at the input to the SUMMER (of Figure 1).

The *only adjustments you should make* during the course of the experiment are to:

- 1. **the step size**: this can be varied in fixed steps with the INTEGRATOR time constant, or fine steps with the gain k of the amplifier (two cascaded BUFFER amplifiers) in the feedback loop (Figure 1).
- 2. *the sampling clock rate*: with the front panel toggle switch of the DELTA MODULATOR UTILITIES module (100, 50, or 25 kHz).

You should keep a record of the waveforms observed. Sketch them all relative to the sampling clock. Make sure each is consistent with expectations before proceeding to the next Task.

Remember the ADDER is modelling the SUMMER (of Figure 1). The two inputs are the message and its approximation. These two should be of the same general shape and the same amplitude. Since it is their difference which is being sought they will need to be of opposite polarity, as has been arranged (remember, the gains **g** and **G** of the ADDER, acting as a SUMMER, have both been set to unity).

Observe the two inputs to the SUMMER. You should use the 'inverse' facility of your oscilloscope (or one channel of another ADDER set to unity gain) and overlay the two displays to simplify their comparison.

warning: remember, when recording other observations, to restore the inverse operation of the oscilloscope to normal

T7 examine the two inputs to the ADDER on CH1-A and CH2-A. These are the input message, and the integrator output respectively. Remember that the integrator waveform is required to be an approximation to the message. Adjust the gain **k** to achieve what you consider the 'best' match. You should have a display similar to that of Figure 2.

You will notice that, despite the fact that the message is a sub-multiple of the clock rate, it is also necessary to fine-tune the oscilloscope sweep speed to obtain a totally stable oscilloscope display. This is through no fault of the oscilloscope - think about it!

T8 find and measure the smallest amplitude step between samples in the INTEGRATOR output waveform over a single clock period. This is the quantizing interval, or step size. Observe that larger steps occur over more than one clock period and that small steps occur when the rate of change of the input is small (near the extrema of the sinewave message). Verify, by calculation, the step size.

Describe in your notes what happens to the approximation when k is decreased, and when k is increased.

T9 observe the ADDER output and confirm that it is the difference between, rather than the sum of, the two inputs. This is the quantizing noise (quantizing error). Notice that not all peaks are of the same height-there are occasional large peaks. Use the WIDEBAND TRUE RMS METER to measure the quantizing noise (remove any DC with the front panel switch). Adjust the step size with the gain k to minimize the quantizing error. Measure the peak-to-peak amplitude, and rms amplitude. Compare with theoretical expectations. Refer Tutorial Ouestion O4.

You will have a chance to measure the distortion of the demodulated signal in the experiment entitled *Delta demodulation* in this Volume. The amount of distortion can be used as another *quantitative* criterion for setting k.

# slope overload

The adjustment of the gain k, as a means of controlling slope overload, has so far been made while watching the INTEGRATOR output. This is a *qualitative* judgement of slope overload.

#### the ADAPTIVE CONTROL signal

In terms of the principle of operation of the delta modulator slope overload gives rise to a succession of samples from the SAMPLER module *of the same sign*. This condition can be detected electronically.

The DELTA MODULATION UTILITIES module has such detection circuitry. When three or more consecutive samples are of the same sign this circuitry signals the fact with a +4 volt output from the ADAPTIVE CONTROL socket of the SAMPLER module. Otherwise the output is at a level of about +2 volt. This signal is used in a later experiment (entitled *Adaptive delta modulation* in this Volume); for now it is instructive to monitor it, for an independent (and more reliable?) indication of slope overload.

T10 vary the gain **k**, and watch the integrator output (CH2-A) for signs of slope overload; at the same time monitor the ADAPTIVE CONTROL signal (CH1-B) and compare its pronouncement with your judgement. Since this is a time-sensitive (phase) measurement, make sure your oscilloscope is set up correctly (eg, not on 'alternate-trace' mode). Record how many clock periods elapse, following the onset of slope overload, before this is signalled by the ADAPTIVE CONTROL output signal.

T11 re-adjust for 'moderate' slope overload. Increase and decrease the step size by means of the INTEGRATOR time constant (SW2A and SW2B on the DELTA MODULATION UTILITIES module circuit board). Confirm that the degree of slope overload changes as expected.

T12 the front panel switch of the DELTA MODULATION UTILITIES module inserts dividers between the clock input and the SAMPLER, to vary the clock rate. Select an intermediate clock rate, and re-adjust for 'moderate' slope overload. Show that slope overload increases when the clock speed is halved, or decreases when the clock rate is doubled. Does the step size change when the clock changes?

### the output

So far you have not looked at the output signal from the modulator! Generally this is the first signal to look at.

The output signal is in TTL format. It is a HI if the INTEGRATOR output is rising, and a LO otherwise. The output signal appears in each of Figures 2,3, 4 and 5.

- T13 use CH1-B to look at the modulator output that is, from the SAMPLER. Compare it with the INTEGRATOR output on CH2-A. Confirm the relationship between the two waveforms.
- T14 observe the relationship between the delta modulator output (CH1-B) and the clock signal (use CH2-B).

So far, as promised, there were only two parameters to be varied during the course of the experiment - the loop gain factor  $\mathbf{k}$ , and the integrator time constant. These were sufficient to allow many observations to be made.

If all of the above has been appreciated it might be a good idea to predict what might happen if the message frequency was changed. Consider the possibilities, then make the change.

- T15 set up as for the conditions of Task T7 (whilst observing the two inputs to the SUMMER).
- T16 set an AUDIO OSCILLATOR to about 2 kHz, and use it for the message (and ext trig signal), instead of the synchronous 2.083 kHz message. Leaving all other variables fixed, vary the message frequency. Whilst it is not easy to stabilise the display, it is still possible to see some consequences, including the onset of slope-overload. Record and explain your observations.

# complex message

A sinewave message is useful for many tests, but a more complex shape can lead to more insights. For meaningful oscilloscope displays it will need to be periodic, and, as before, a sub-multiple of the sampling rate.

Such a message is easy to make with TIMS; a possible method is described in the Appendix to this experiment.

Such a message was used to produce the waveforms of Figures 3, 4, and 5.

T17 make a synchronous, complex message. Vary its shape, and observe results under different conditions.

# **TUTORIAL QUESTIONS**

- **Q1** why is it useful to set up the experiment using the 2 kHz signal from the MASTER SIGNALS module, as opposed to a signal from an AUDIO OSCILLATOR, for example?
- **Q2** what are the system parameters which control the step size (quantization amplitude) for a given sampling rate?
- Q3 knowledge of the step size alone is insufficient to make a statement about the possibility of slope overload. What else needs to be known?
- **Q4** calculate the peak-to-rms ratio of a constant peak-to-peak amplitude sawtooth waveform.
- **Q5** show that delta modulation is a special case of differential pulse code modulation (DPCM). What is the number of bits per word?

### **APPENDIX**

# a 'complex' message.

We can define a 'complex' message as one which is periodic, and having a shape exhibiting more slope changes than a pure sinewave. As an example, see Figure A.1.

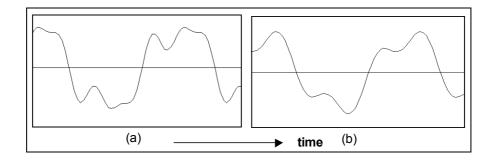


Figure A1: two 'complex' messages

Such a message can be made by filtering a square wave.

The square wave can be obtained by passing a sinewave through a comparator. The TIMS COMPARATOR has an analog output. Its limiting characteristic can be set to 'hard' <sup>1</sup>. See the *TIMS User Manual*. The amplitude limited output contains odd harmonics, and the first two or three can be filtered off (together with the fundamental) to make the new shape.

By including a PHASE SHIFTER (this introduces a phase shift which varies with frequency), the shape can be further modified; but this is not essential.

For synchronous displays, in the present experiment, it is useful to use the 2.083 kHz MESSAGE from MASTER SIGNALS.

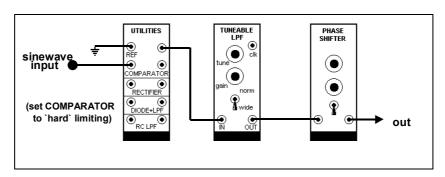


Figure A2: a 'complex' message generator

The waveforms of Figure A1 were made by selecting the first three odd harmonics (a), and the first two odd harmonics (b) respectively. Many shape variations are possible, including these, as the phase is varied.

<sup>&</sup>lt;sup>1</sup> SW1 toggles DOWN; SW2 toggles UP

An interesting feature is that, by obtaining the complex waveform shape with the TUNEABLE LPF in the WIDE mode, instant reversion to a sine wave is effected by toggling to the NORM mode.